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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,822	03/06/2002	Kenji Furuya	1614.1221	5676

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EXAMINER

DANG, KHANH NMN

ART UNIT	PAPER NUMBER
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2111

DATE MAILED: 07/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/090,822

Applicant(s)

FURUYA ET AL.

Examiner

Khanh Dang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>20020509</u> . | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Nozuyama (5,862,359).

At the outset, it is noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted, these claims do not define any structure that differs from Nozuyama.

With regard to claims 1 and 10, Nozuyama discloses a semiconductor device (10, for example) comprising: a plurality of function blocks (13, 14, 15, and 16, for example); a plurality of buses (22, 23, for example), each of which is respectively connected to one of the plurality of function blocks (13, 14, 15, 16); a plurality of control signal lines (EN12-EN31, see also column 6, lines 1-46), each of which is respectively connected to one of the plurality of function blocks (13-

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16); a main bus (21, connected to CPU 11); a bus control unit (CPU 11) connected to the main bus (21); a bus division control unit (including 3 and 4) located between the plurality of buses and the main bus (21), for connecting one of the plurality of buses (22, 23) to the main bus (21) and transmitting a control signal to a corresponding one of the plurality of control signal lines (EN12-EN31, see also column 6, lines 1-46) in accordance with a decoded result of information supplied from the bus control unit via the main bus (21), thereby controlling a corresponding one of the plurality of function blocks and controlling communication between at least two functional blocks (see at least column 3, lines 18-23; column 7, lines 10-19).

With regard to claim 2, the bus division control unit comprises: a decoder unit (4) for decoding the information supplied from the bus control unit (11) via the main bus (21) and generating the control signal; and a bus dividing unit (see Figs. 2A/2B, column 6, lines 1-46) for connecting one of the plurality of buses to the main bus, in accordance with a decoded result of the decoder unit.

With regard to claim 3, the bus division control unit (including 3 and 4) connects one of the plurality of buses (22, 23) to the main bus (21), in accordance with a decoded result of address information (address of the functional unit that the CPU needs to access must be always provided by the CPU) transmitted from the bus control unit via the main bus (see at least column 3, lines 18-23; column 7, lines 10-19).

With regard to claim 4, at least two of the plurality of function blocks (13, 14, for example) shares one (22, for example) of the plurality of buses, and the bus division control unit (including 3 and 4) controls a transfer operation between the two function blocks (13, 14) via the one (22) of the plurality of buses in response to a transfer request signal.

With regard to claim 5, it is clear that the bus division control unit (including 3 and 4) simultaneously transmits a write-enable signal to one of the two function blocks and a read-enable signal to the other one of the two function blocks (in Nozuyama, as discussed above, the communication, i.e., read/write, between functional blocks 13 and 14 is enabled by an enable signal from bus switch 3; blocks 13 and 14 receive the signal simultaneously and one of the functional blocks (13, 14) reads the other one of blocks (13, 14) writes.

With regard to claim 6, it is clear that in order to enable communication between the blocks (13, 14, for example), the source (either 13 or 14) and the destination (the other of 13 or 14) must be specified/determined.

With regard to claim 7, as in any master/initiator and slave/target relationship, in Noyuyama, the CPU has to send request access (by specifying the address of the target or functional unit) for processing before the actual transfer request may be processed by the bus division control unit including the bus switch 3 and the decoder 4.

With regard to claim 8, it is clear that when access request to blocks 13, 14, for example is granted and transfer is processed, the CPU 11 can make

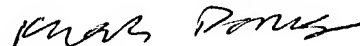
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another access request to functional blocks 15 and 16 while the transfer is in progress.

With regard to claim 9, in Nozuyama, the CPU can make either a READ or WRITE request to the functional blocks, and the bus switch (3) and decoder (4) must be able to recognize the type of request in accordance to the principle of computer architecture so that a suitable communication direction between the CPU and the plurality of functional blocks can be performed.

U.S. Patent No. 6,662,260 to Wertheim et al. is of particular interest. Wertheim et al. discloses a plurality of functional blocks interconnected by a bus, a switch controller partitioning the bus into a plurality of bus segment and controlling the two of the bus segments so that the two bus segment can be interconnected or isolated in response to control information representative of the source and the destination of each bus transaction. The switch controller can also control the state of the switches to permit two or more bus transaction to be performed simultaneously.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.



Khanh Dang
Primary Examiner